

MS-7680 Ver: 2.0 m-ATX : 245 X 215mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot * 1

PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI *1

TPM Header *1

COM Header *1

LPT Header *1

on BOARD BUZZER

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三個BOM:

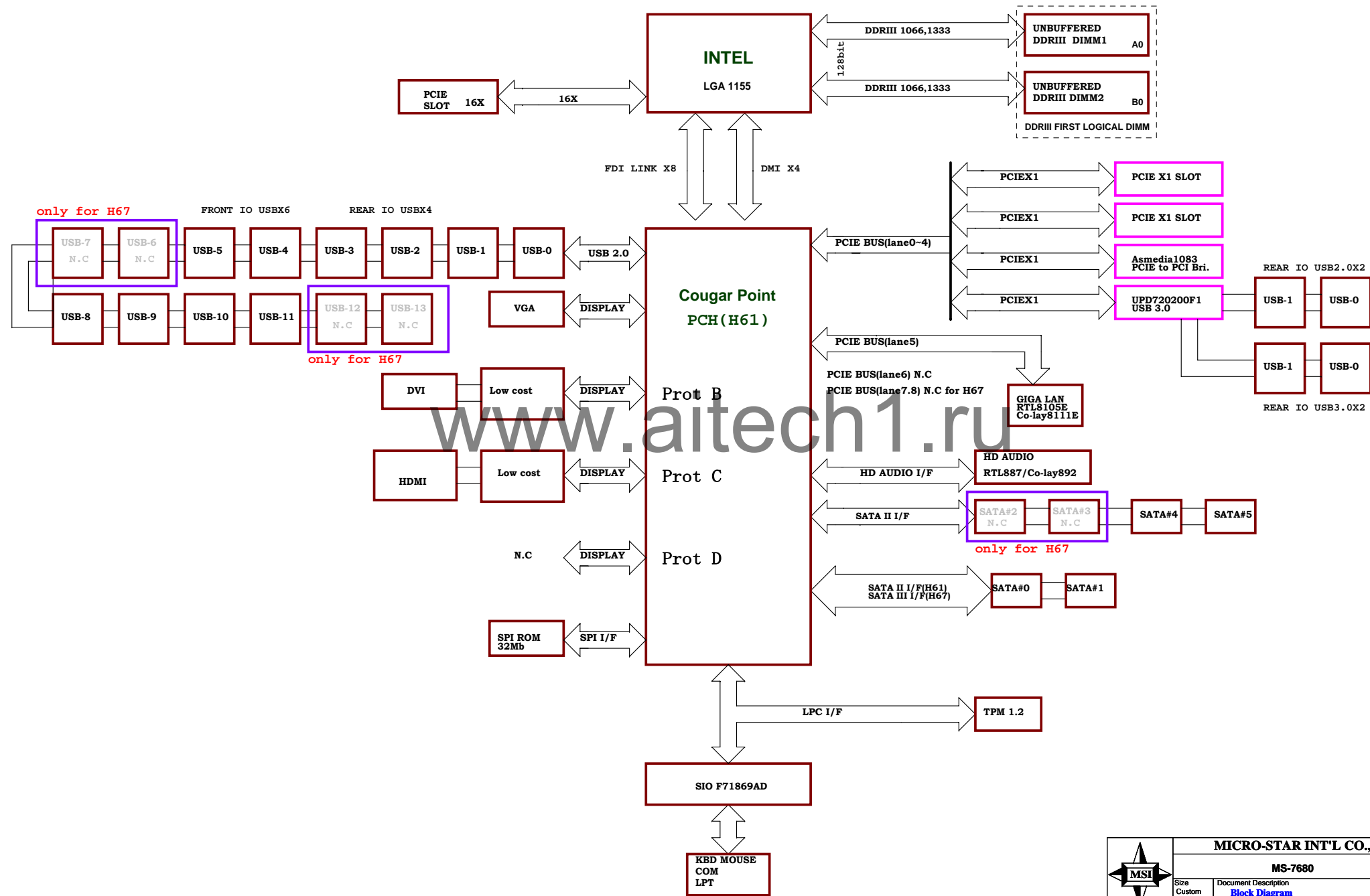
- 1.H67 Full Spec(全固)
- 2.H61 Full Spec(全固)
- 3.H61 common Spec(半固)

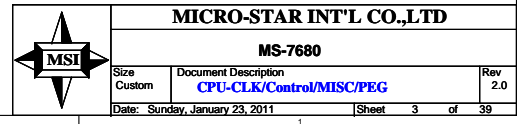


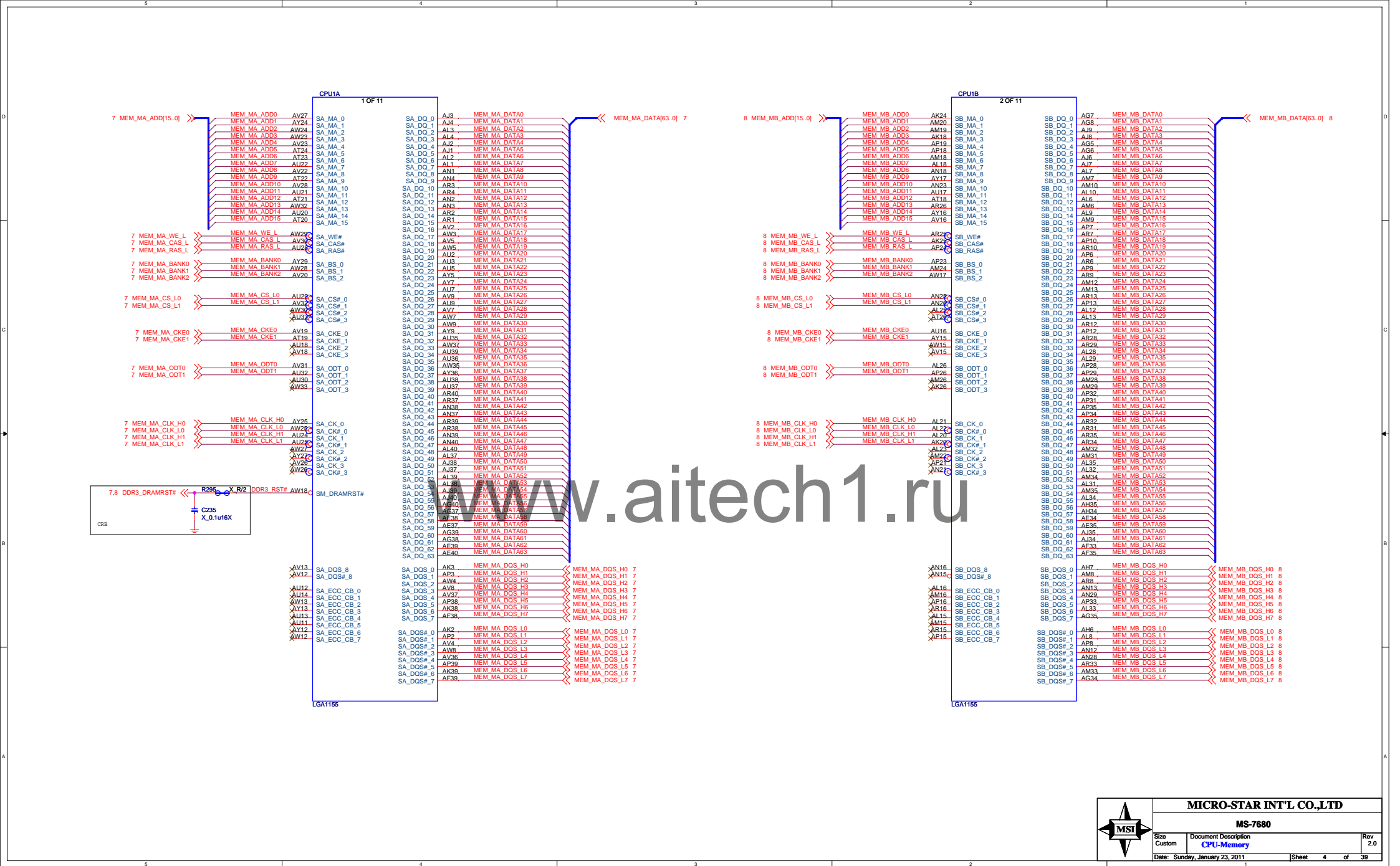
MICRO-STAR INT'L CO.,LTD

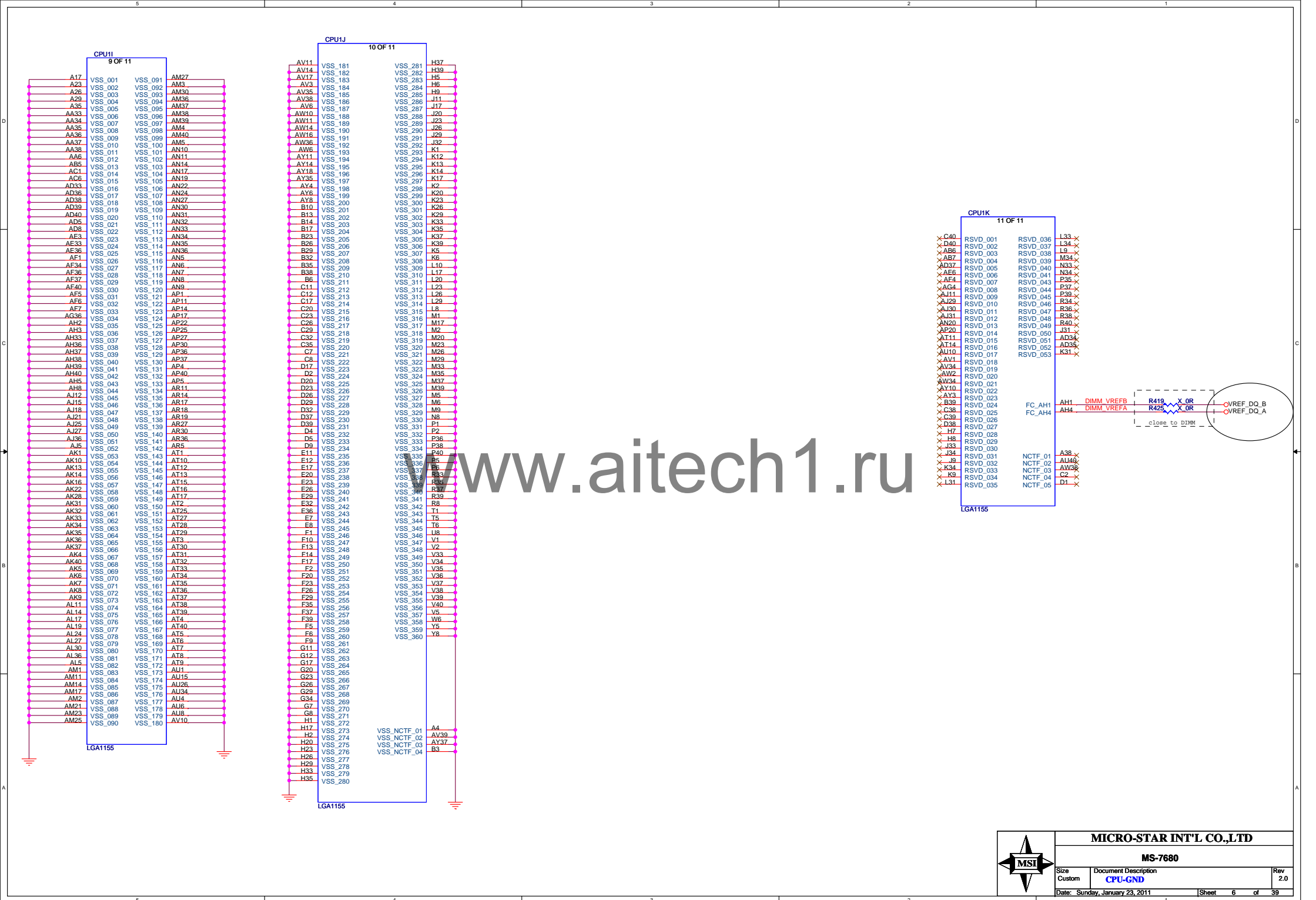
MS-7680

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| Size Custom | Document Description Cover Sheet | Rev 2.0 |
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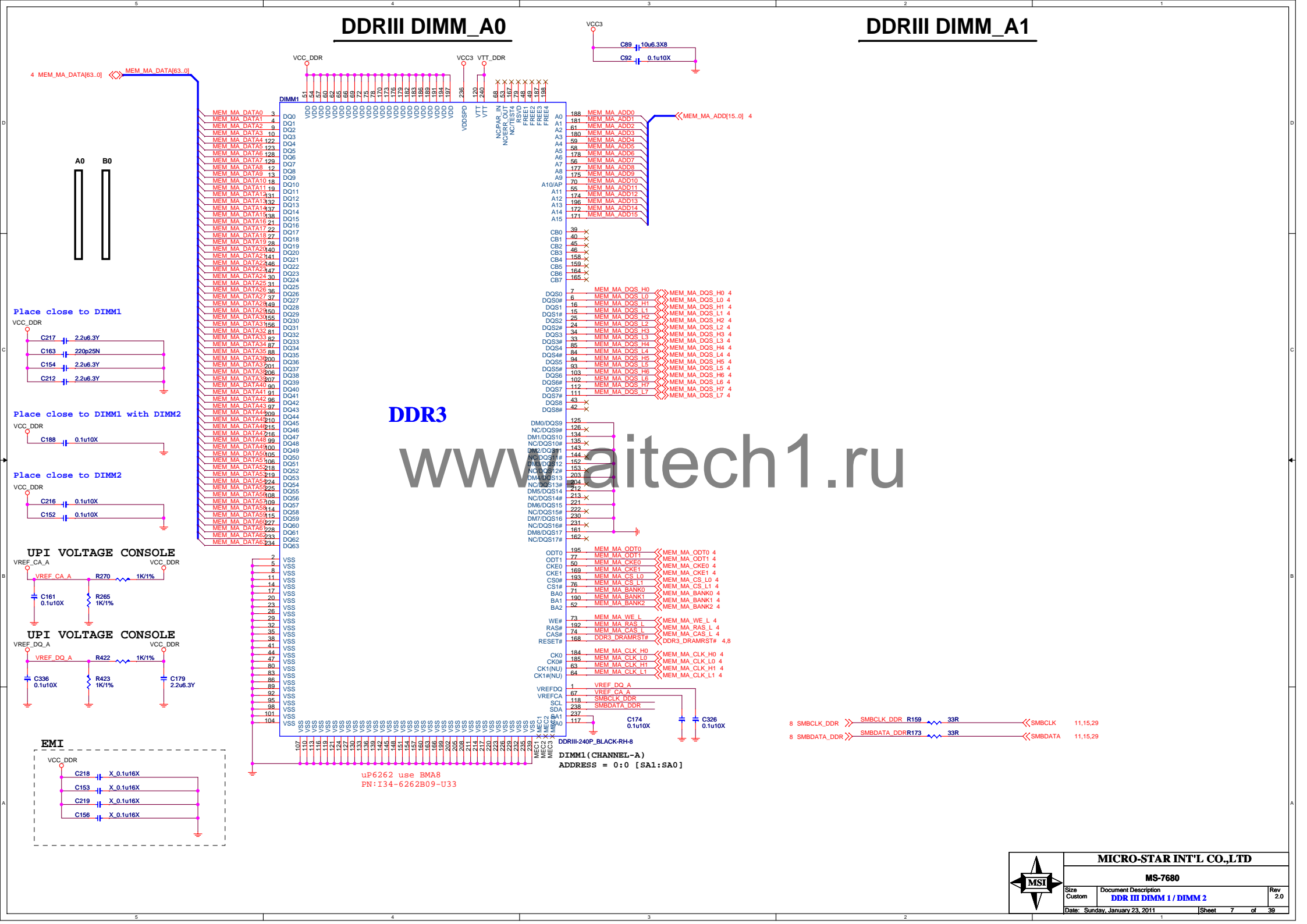


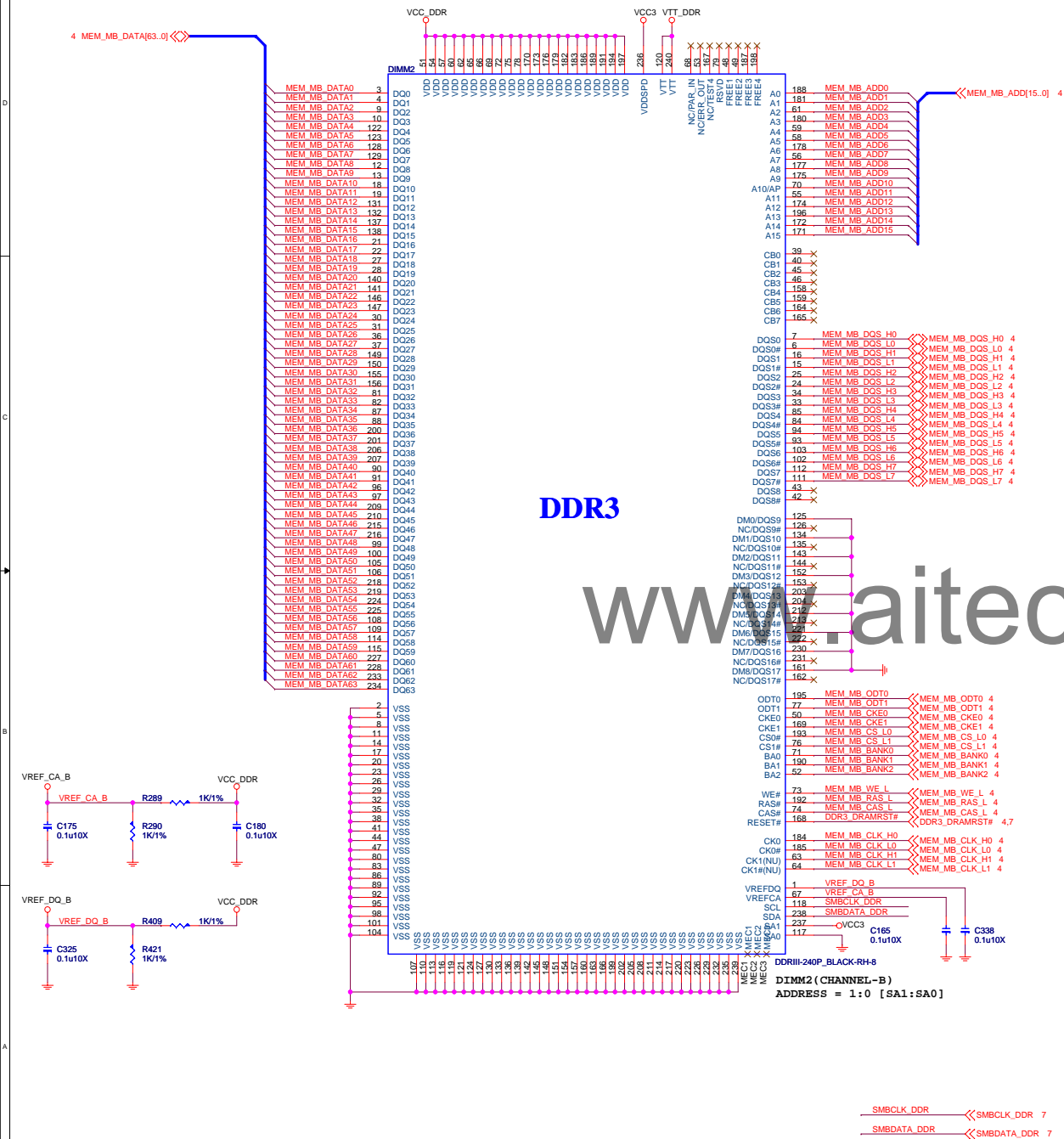


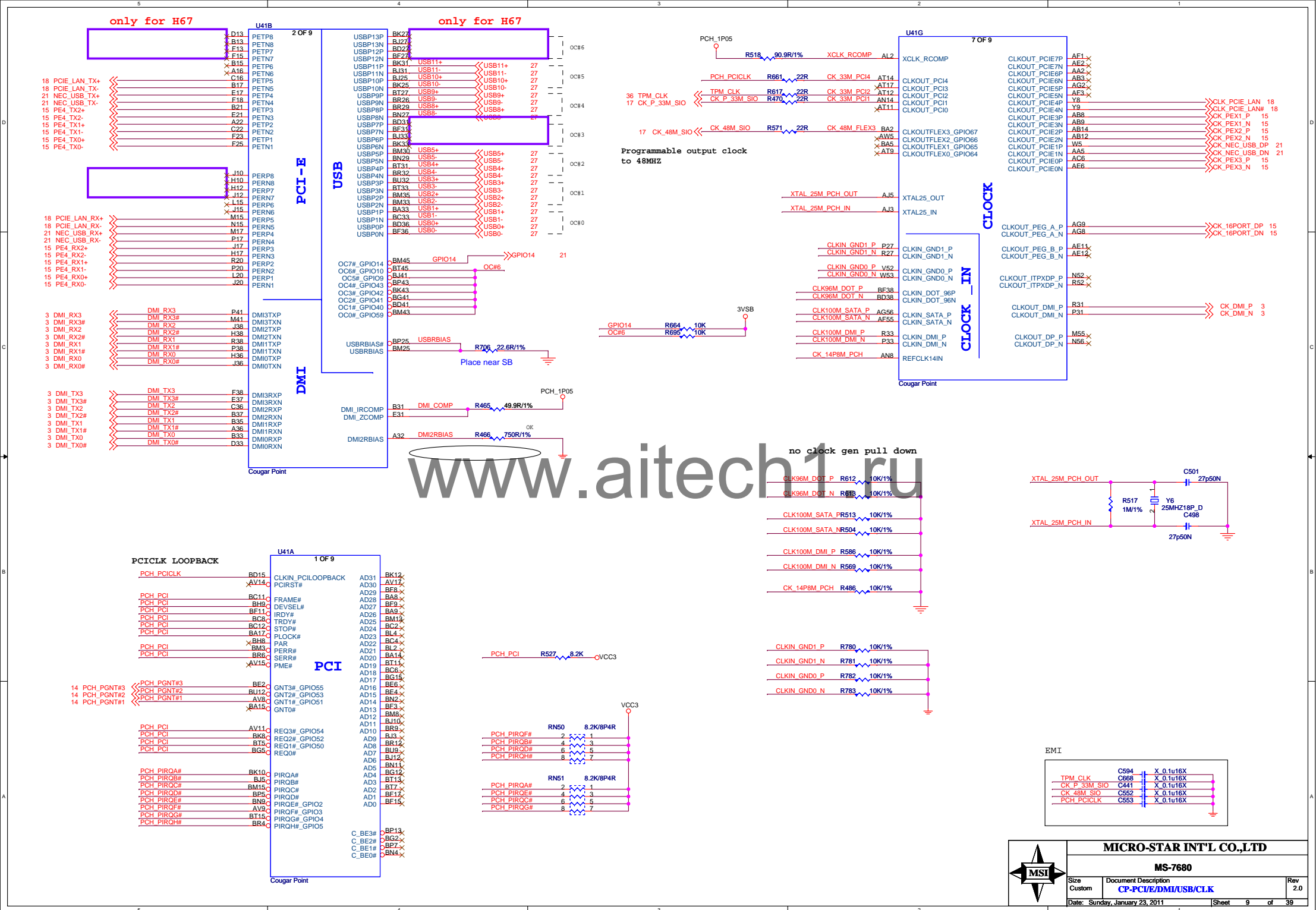


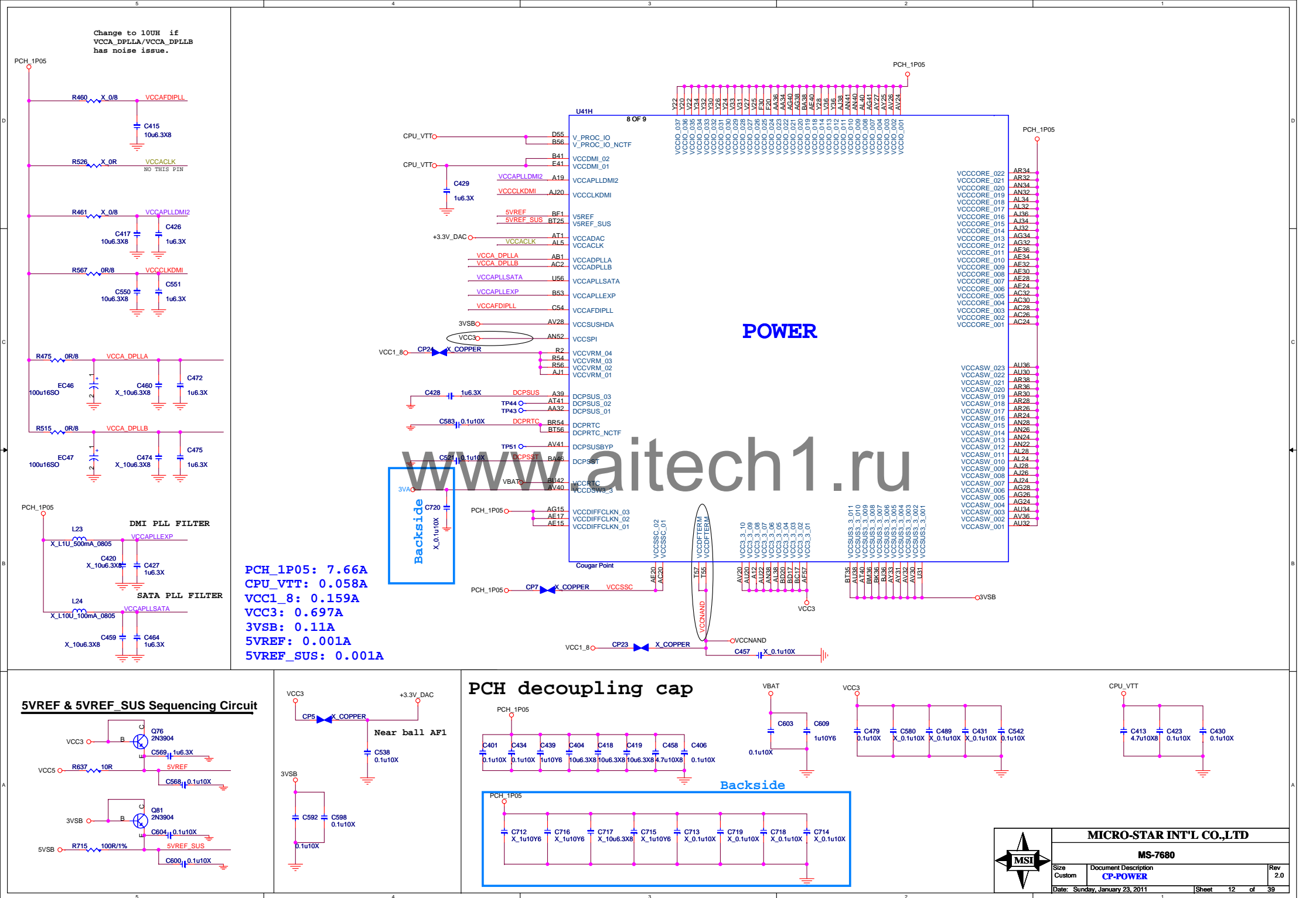
DDRIII DIMM_A0

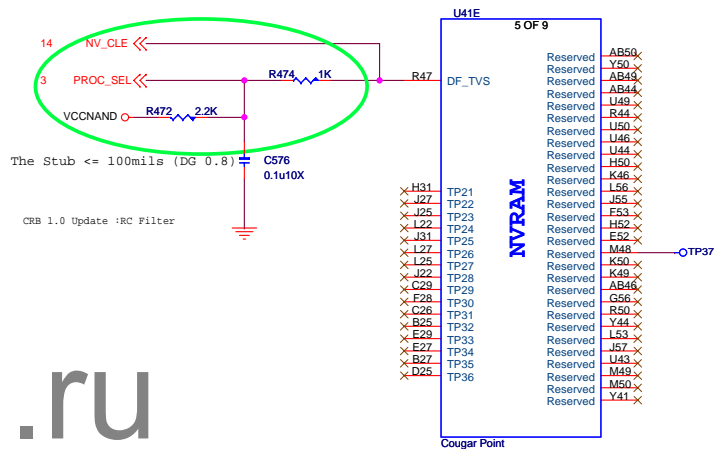
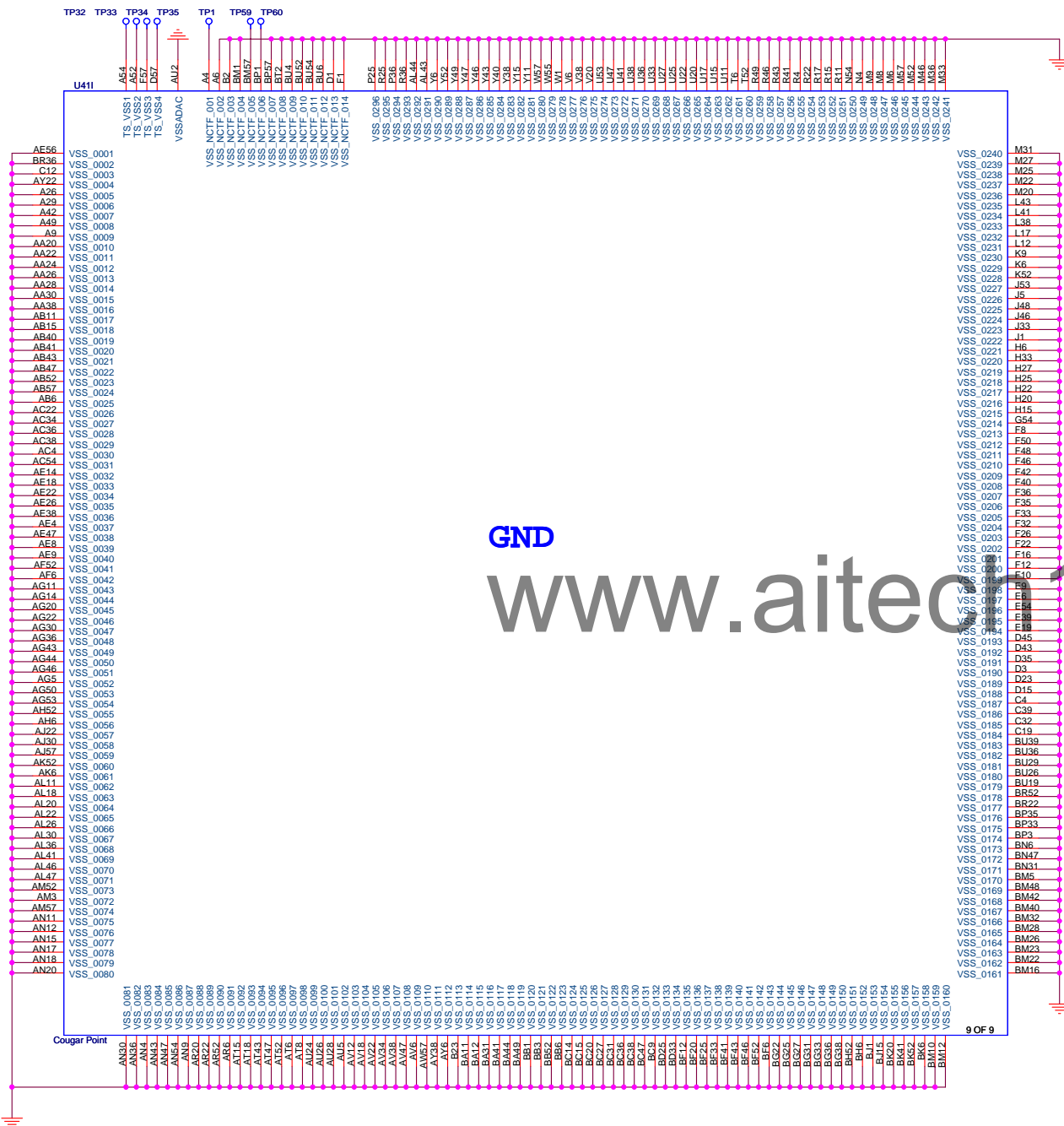
DDRIII DIMM_A1





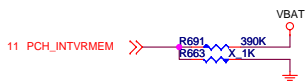
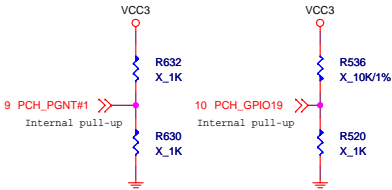






PCH Straps

| BOOT DEVICE | GNT1 | SATA1GP/GPIO19 |
|-------------|------|----------------|
| LPC | 0 | 0 |
| PCI | 1 | 0 |
| SPI | 1 | 1 |



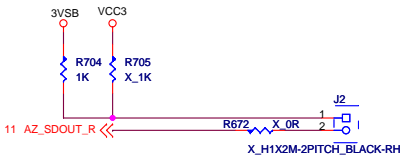
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



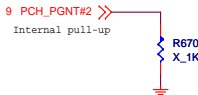
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.

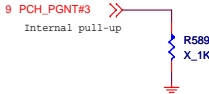


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

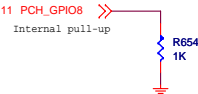
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



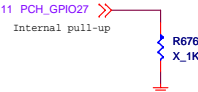
DMI AC/DC MODE
0 : AC
1 : DC *



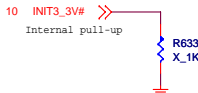
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

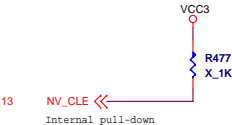
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



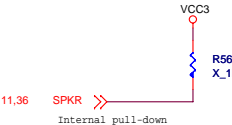
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY*
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



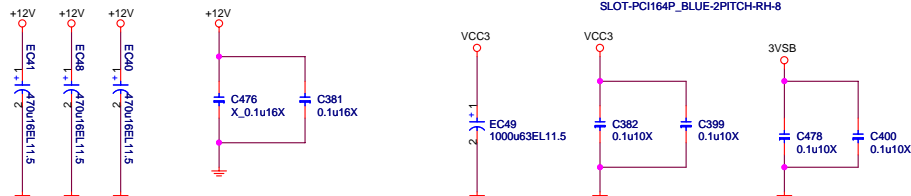
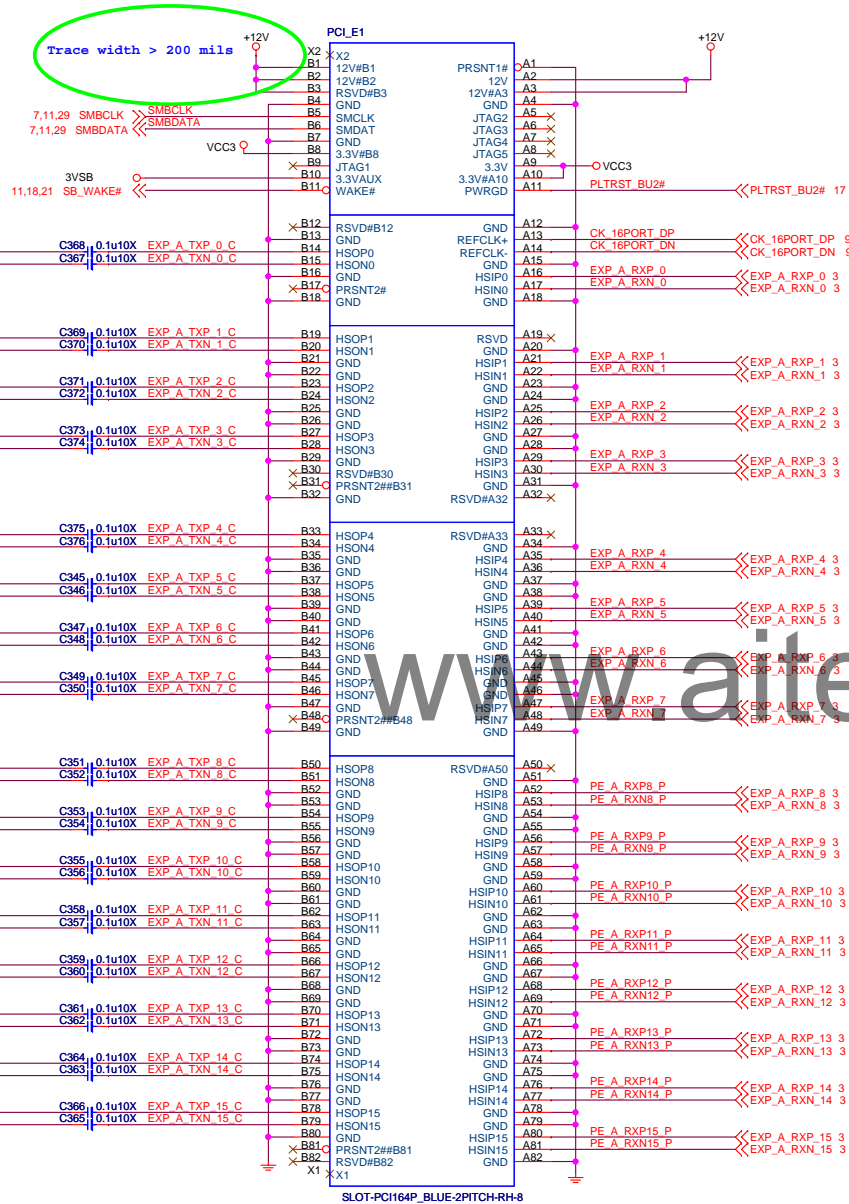
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



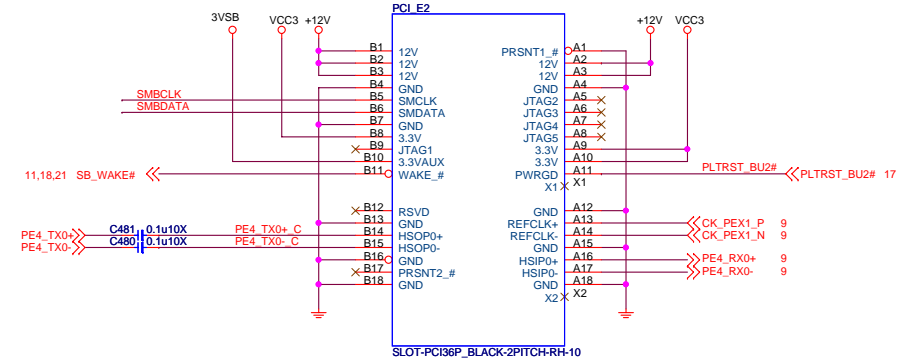
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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| MICRO-STAR INT'L CO.,LTD | | |
| MS-7680 | | |
| Size | Document Description | Rev |
| Custom | CP-Strap | 2.0 |
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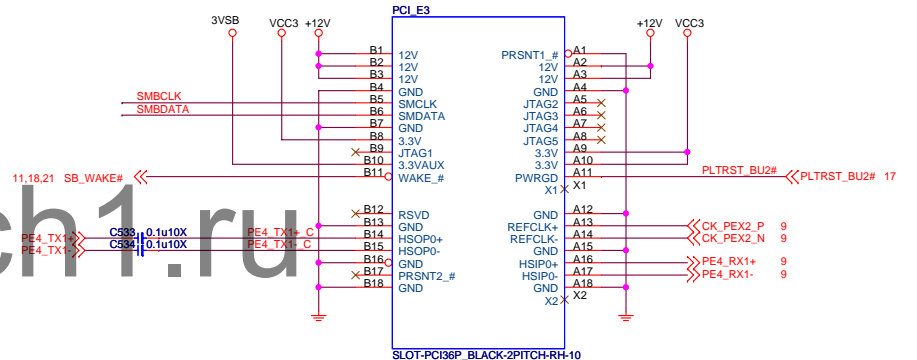
PCI_Express X16 slot



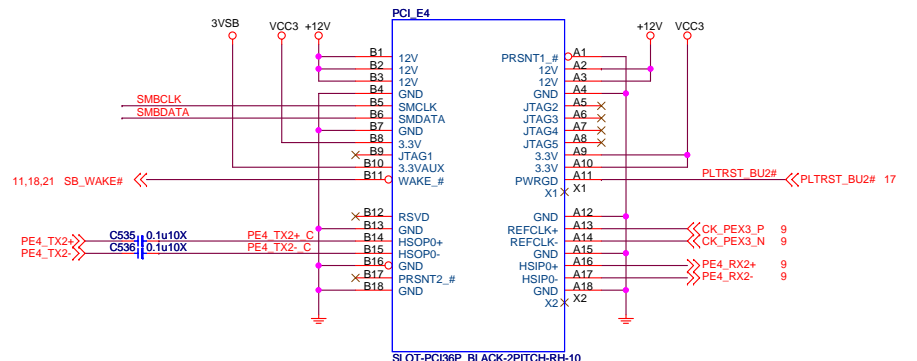
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT




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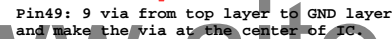
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| Size | Document Description | Rev |
|--------------------------------|----------------------|-----|
| Custom | PCIe x16 x1/x1 | 2.0 |
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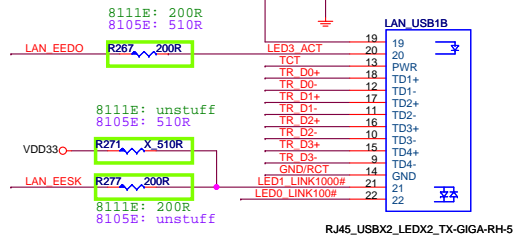
| | | | | |
|---|----------------------|-------|--------------------------|-------|
|  | | | MICRO-STAR INT'L CO.,LTD | |
| | | | MS-7680 | |
| Size | Document Description | | | Rev |
| Custom | PCx1 Slots | | | 2.0 |
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RTL8105E 10/100M LAN



Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

The diagram shows a section of a PCB layout. A horizontal line represents a trace. Below it, a vertical line connects to a circular pad. This pad is labeled 'VDD33'. To the right of this pad, there is a label 'LAN Connector' with a horizontal line pointing to it. Below the 'LAN Connector' label, there is a label 'GND' with a horizontal line pointing to it. A vertical line connects the 'VDD33' pad to the 'GND' pad. A small circle is located on the vertical line between the two pads, with a label '9 via from top layer to GND layer' pointing to it. The text 'and make the via at the center of IC.' is also present.

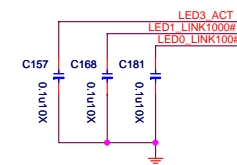










| | 3.3V | mW |
|-----------------|-------|---------|
| 10 M Idle/TxRx | 14/75 | 46/248 |
| 100 M Idle/TxRx | 43/66 | 142/218 |
| S0 ALDPS | 3.2 | 11 |

| | 3.3V | mW |
|-----------------|---------|---------|
| 10 M Idle/TxRx | 12/66 | 40/218 |
| 100 M Idle/TxRx | 31/44 | 102/145 |
| Giga Idle/TxRx | 135/163 | 452/538 |
| ALDPS | 4 | 13 |

| | 3.3V | mW |
|-----------------|---------|---------|
| 10 M Idle/TxRx | 12/66 | 40/218 |
| 100 M Idle/TxRx | 31/44 | 102/145 |
| Giga Idle/TxRx | 135/163 | 452/538 |
| ALDPS | 4 | 13 |

| | 3.3V | mW |
|-----------------|---------|---------|
| 10 M Idle/TxRx | 12/66 | 40/218 |
| 100 M Idle/TxRx | 31/44 | 102/145 |
| Giga Idle/TxRx | 135/163 | 452/538 |
| ALDPS | 4 | 13 |



| Giga-Lan | | 10/100-Lan | |
|---|---|---|---|
| N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None | | N58-22F0771 Link Yellow Active Blinking 100 Green 10 None | |
| 19 ————— 20 ————  ———— Yellow |  | 19 ————— 20 ————  ———— Yellow |  |
| 21 ————— Orange | | 21 ————— | |
| 22 ————  ———— Green |  | 22 ————  ———— Green |  |

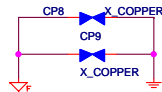
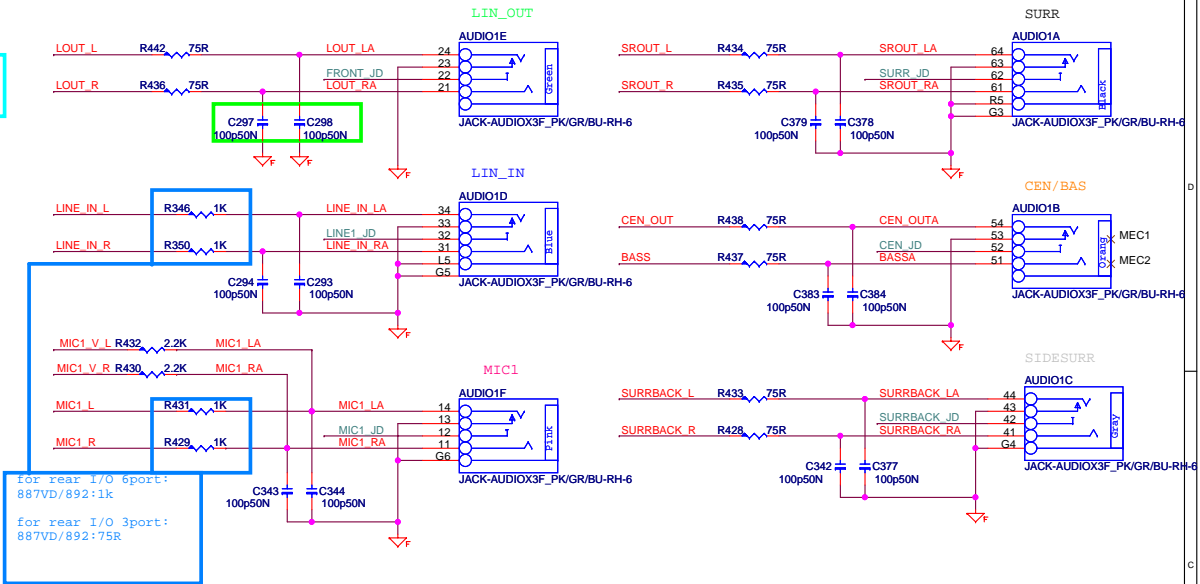


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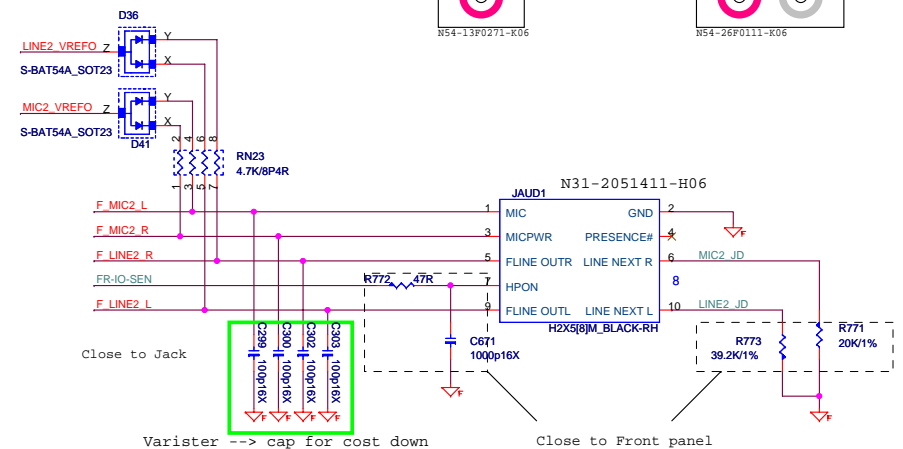
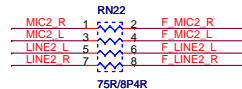
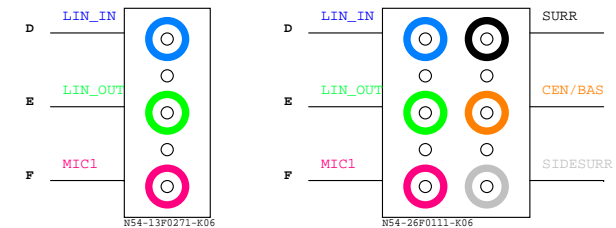
MS-7680

| | | |
|--------------------------------|---|----------------|
| Size Custom | Document Description LAN - RTL8111E / 8105E | Rev 2.0 |
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ALC892



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MS-7680

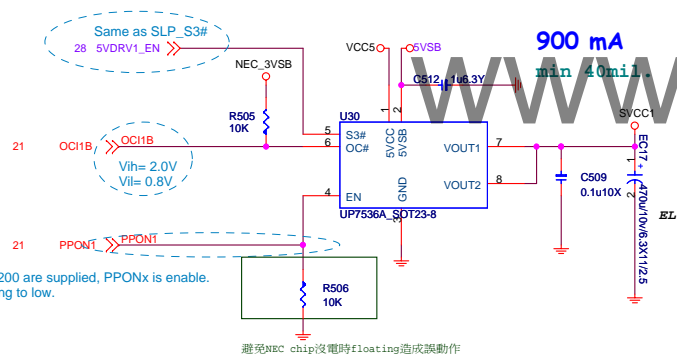
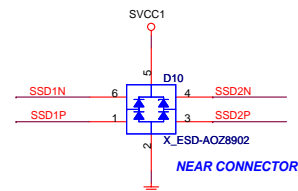
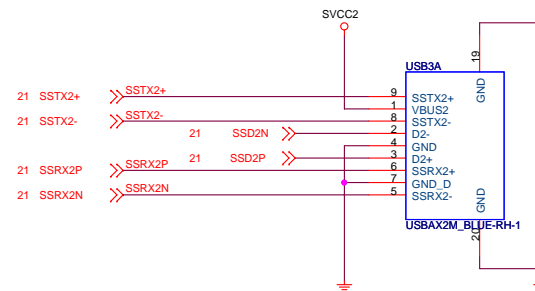
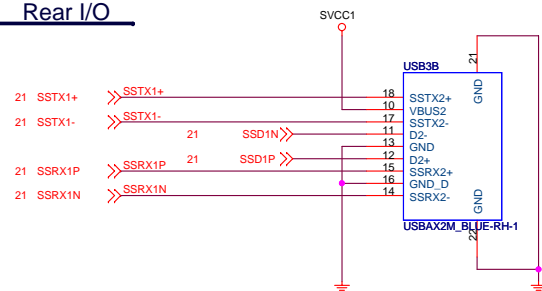
| | | |
|--------------------------------|--|----------------|
| Size Custom | Document Description ALC892_COLAY_ALC887VD | Rev 2.0 |
| Date: Sunday, January 23, 2011 | | Sheet 19 of 39 |

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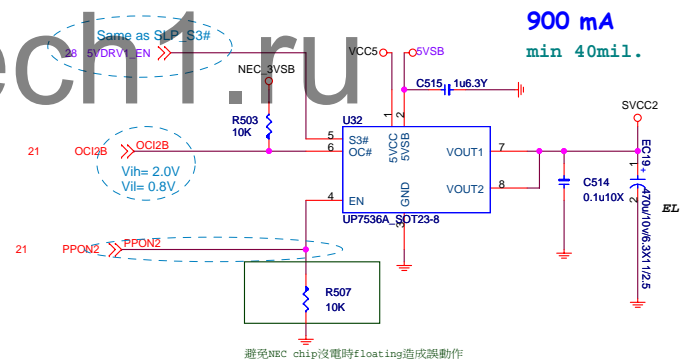
| | | |
|--------------------------------|--|----------------|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-7672 | | |
| Size Custom | Document Description ASM1083 PCI Brl. | Rev 2.0 |
| Date: Sunday, January 23, 2011 | | Sheet 20 of 39 |

Rear I/O



All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OC1x going to low.

避免NEC chip沒電時floating造成誤動作



避免NEC chip沒電時floating造成誤動作

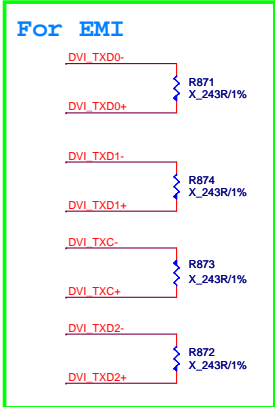


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MS-7672

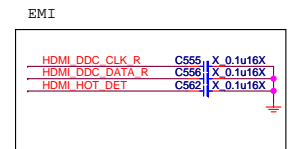
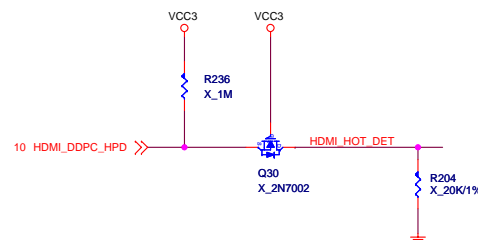
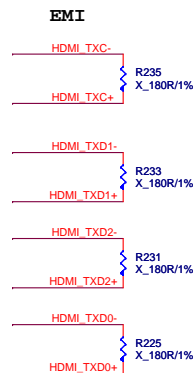
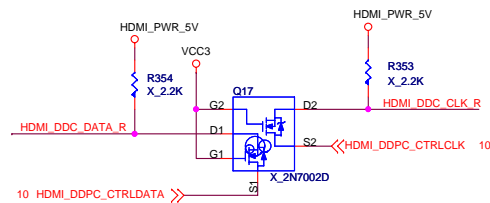
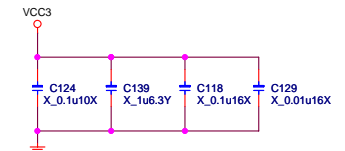
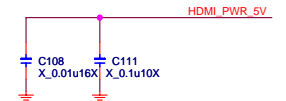
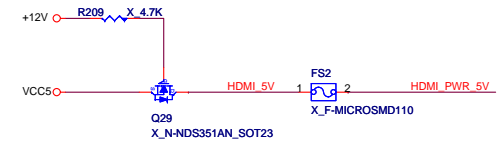
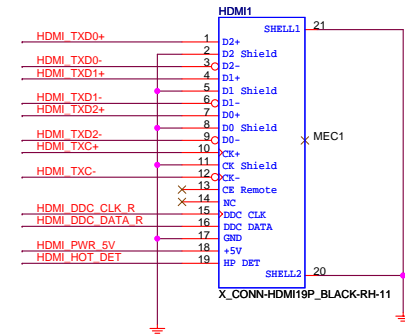
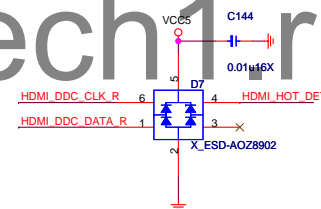
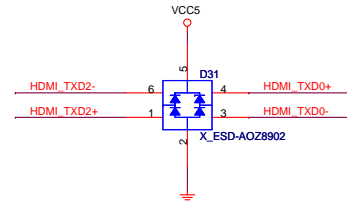
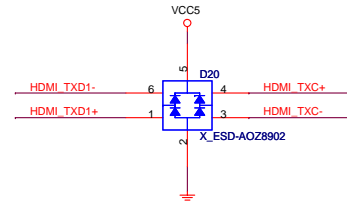
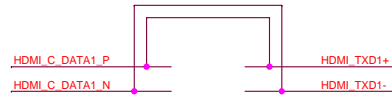
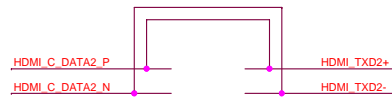
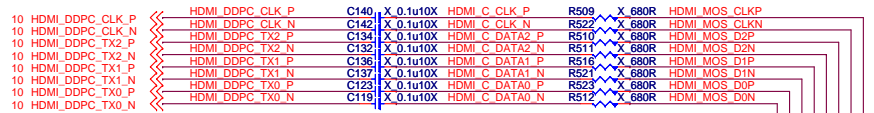
| | | |
|--------------------------------|--|----------------|
| Size Custom | Document Description USB 3.0 Power & Connector | Rev 2.0 |
| Date: Sunday, January 23, 2011 | | Sheet 22 of 39 |

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI level shifter

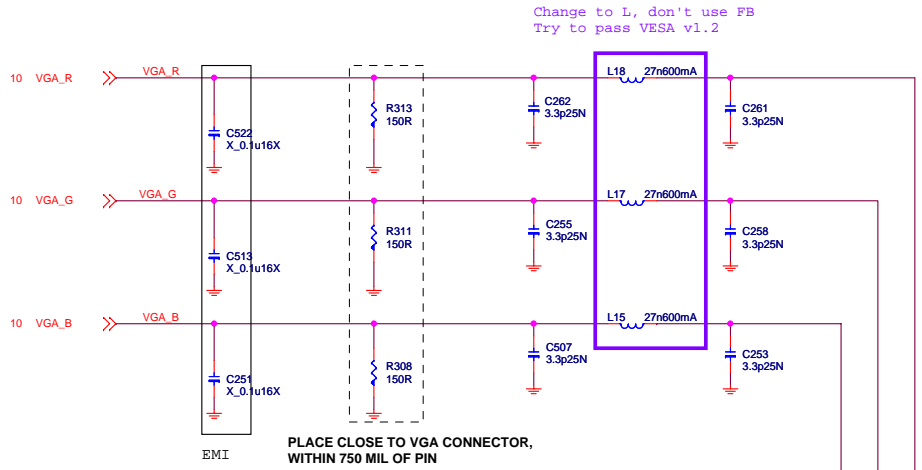
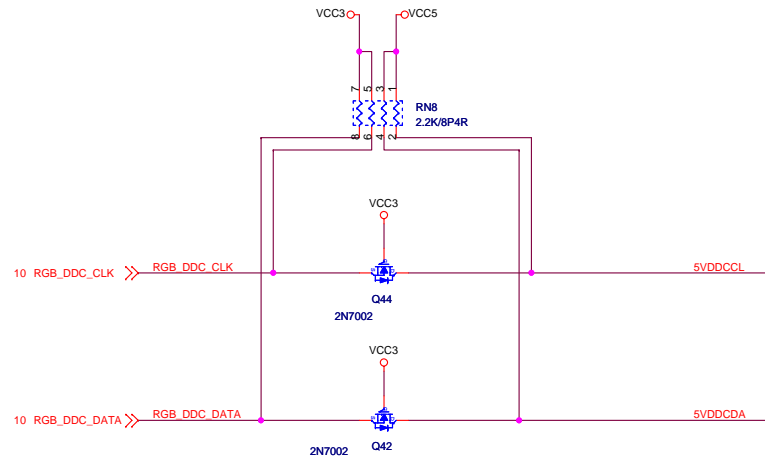
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



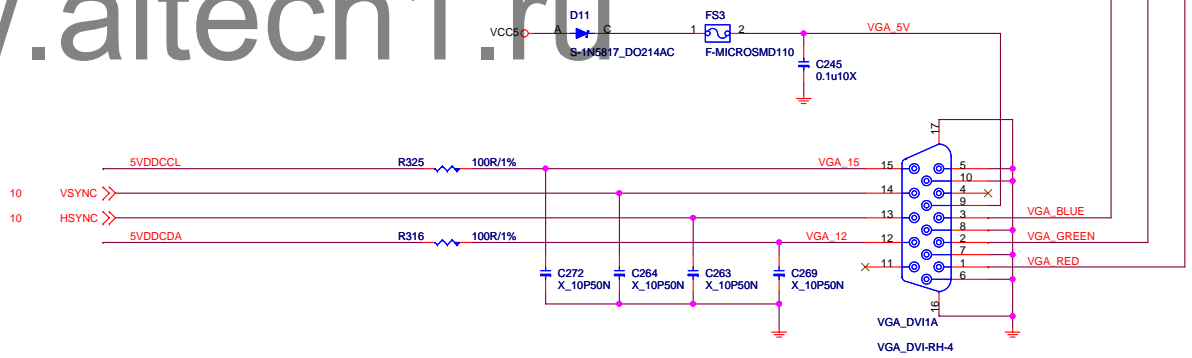
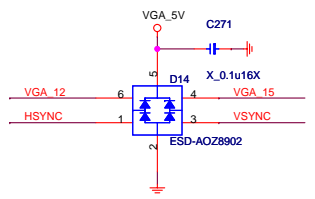
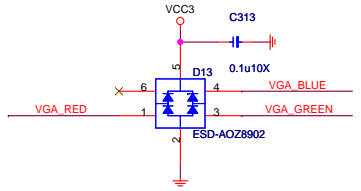
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

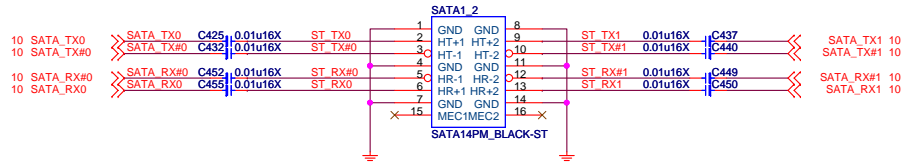


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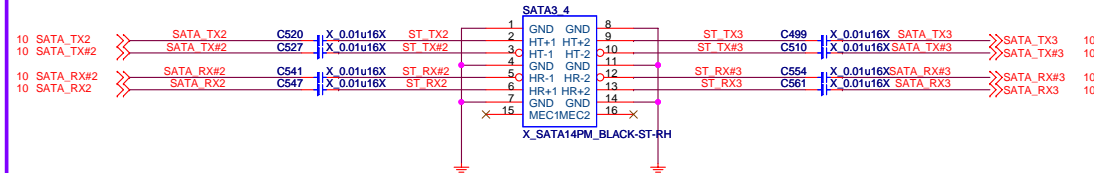


SATA 6G PORT 0,1

H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G



SATA 3G PORT 2,3

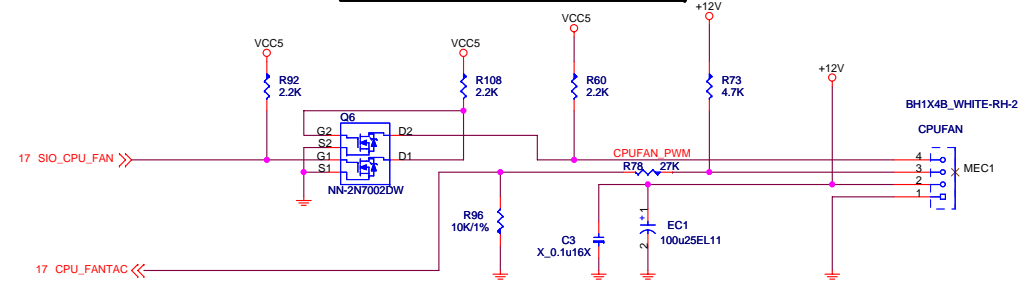


For H61,SATA3&4 removed

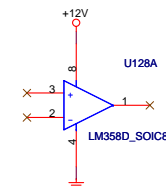
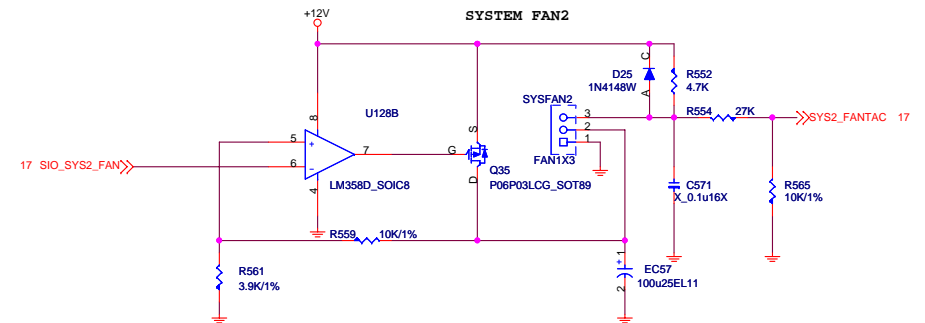
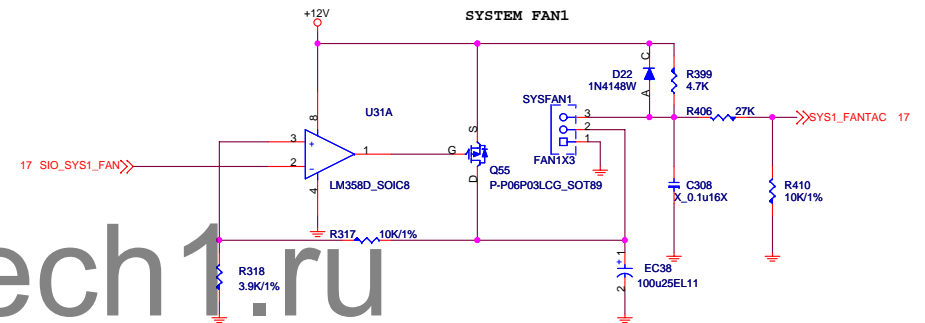
www.aitech1.ru



CPU FAN-COUNTROL CIRCUIT

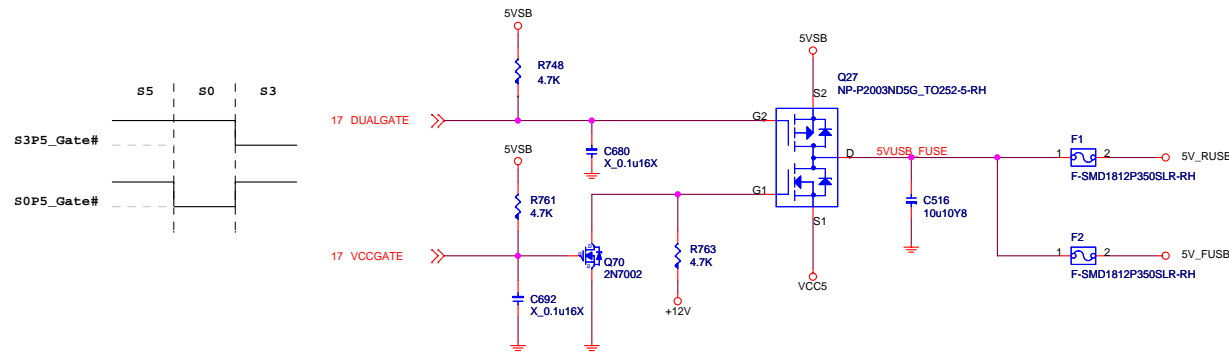


SYSTEM FAN-COUNTROL CIRCUIT



| MICRO-STAR INT'L CO.,LTD | | | |
|--------------------------|--------------------------|-------|----------|
| MS-7680 | | | |
| Size | Document Description | Rev | |
| Custom | SATA / FAN Control | 2.0 | |
| Date: | Sunday, January 23, 2011 | Sheet | 26 of 39 |

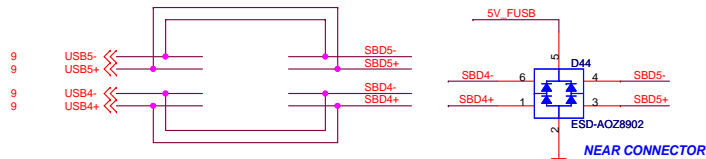
5V_RUSB Switch



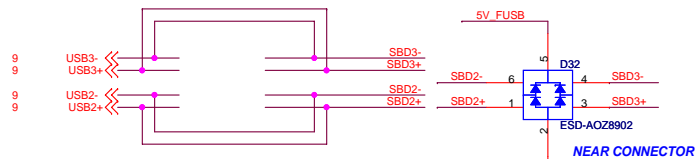
Front USB Connector

For H61 6,7,12,13 Port should be remove

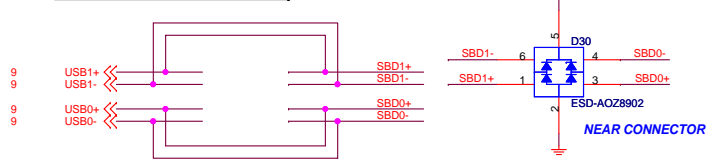
FRONT USB PORT 4,5



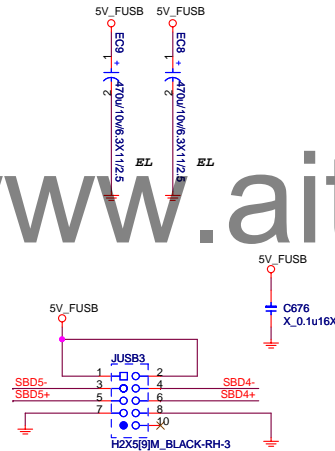
FRONT USB PORT 2,3



FRONT USB PORT 0,1

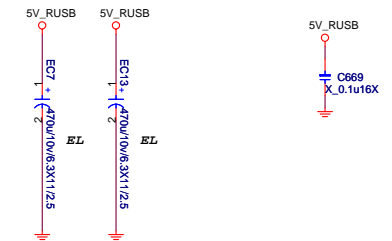


NEAR USB Front CONNECTOR

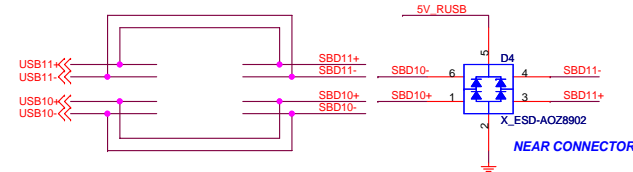


Rear USB Connector

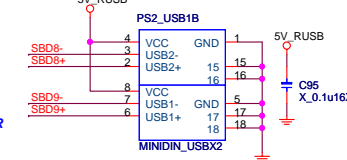
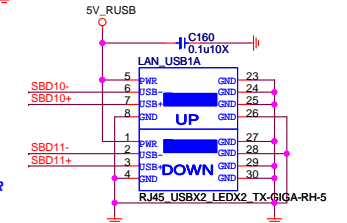
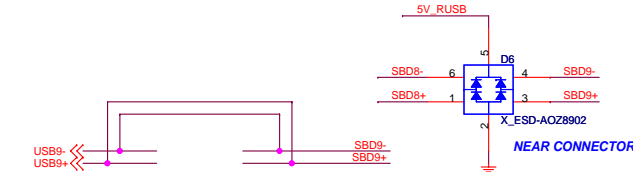
NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)

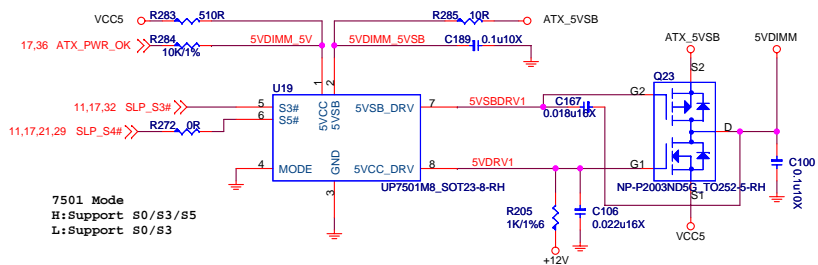


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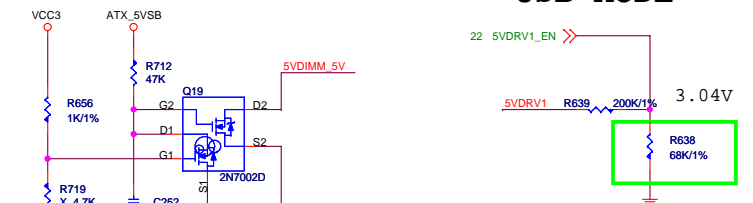
MS-7680

| Size | Document Description | Rev |
|--------------------------------|----------------------|-----|
| Custom | USB Connector | 2.0 |
| Date: Sunday, January 23, 2011 | Sheet 27 of 39 | |

5VDIMM FOR DDR



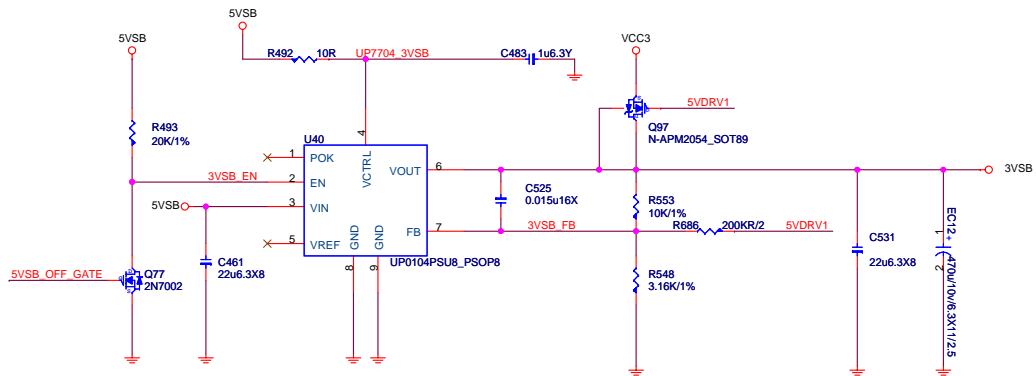
USB MODE



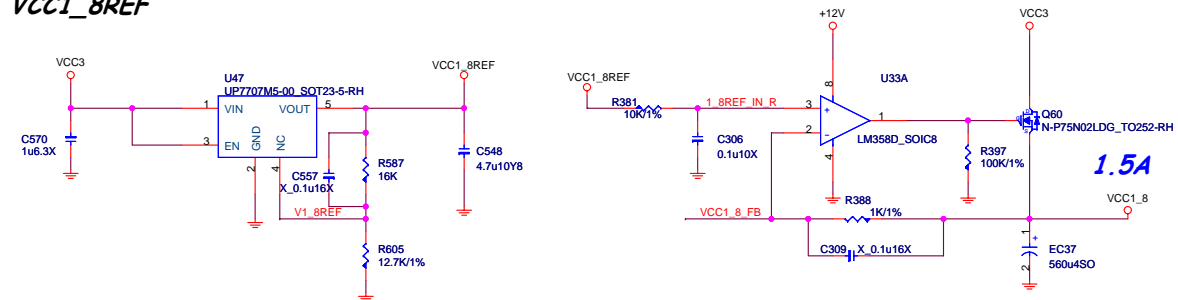
Patch coolermaster 700w power sequence

3VSB

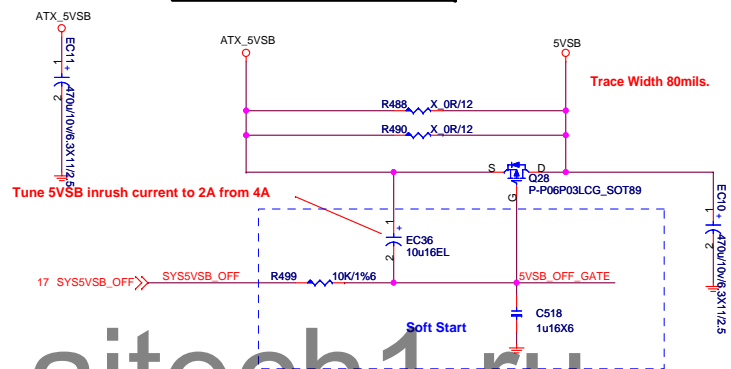
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



VCC1_8REF



5VSB Power Switch



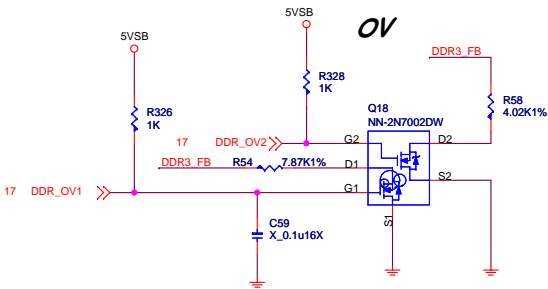
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DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU

7.5A FOR 2DIMM

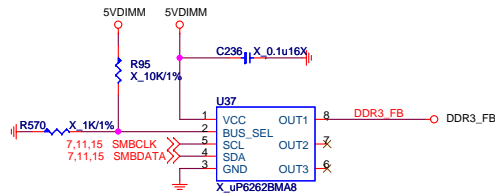
1A FOR DDR VTT



*Default 1.5V

| | | | | |
|---------|-------|------|-------|------|
| DDR_OV | 1.35V | 1.5V | 1.65V | 1.8V |
| DDR_OV1 | Low | High | Low | High |
| DDR_OV2 | Low | Low | High | High |

DDR_OV1 = GPIO01 (S/I/O)
DDR_OV2 = GPIO02 (S/I/O)

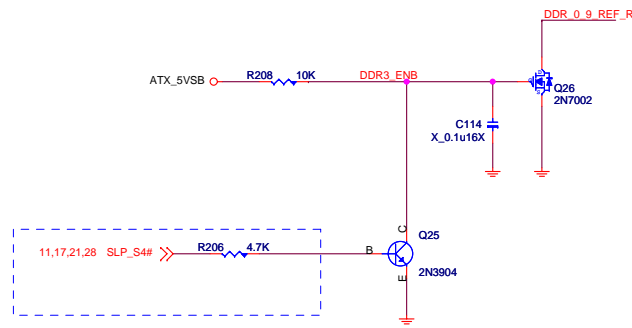


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

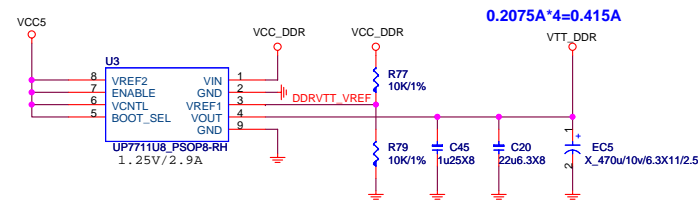
| ADDRESS | 0x2A | 0x28 | 0x26 | 0x24 | 0x22 | 0x20 |
|-----------|------|------|------|------|------|------|
| RH (KOhm) | OPEN | 3.9 | 3 | 2.2 | 1.3 | 10 |
| RL (KOhm) | 10 | 1.3 | 2.3 | 3 | 3.9 | OPEN |
| BUS_SEL | 0% | 25% | 40% | 60% | 75% | 100% |

P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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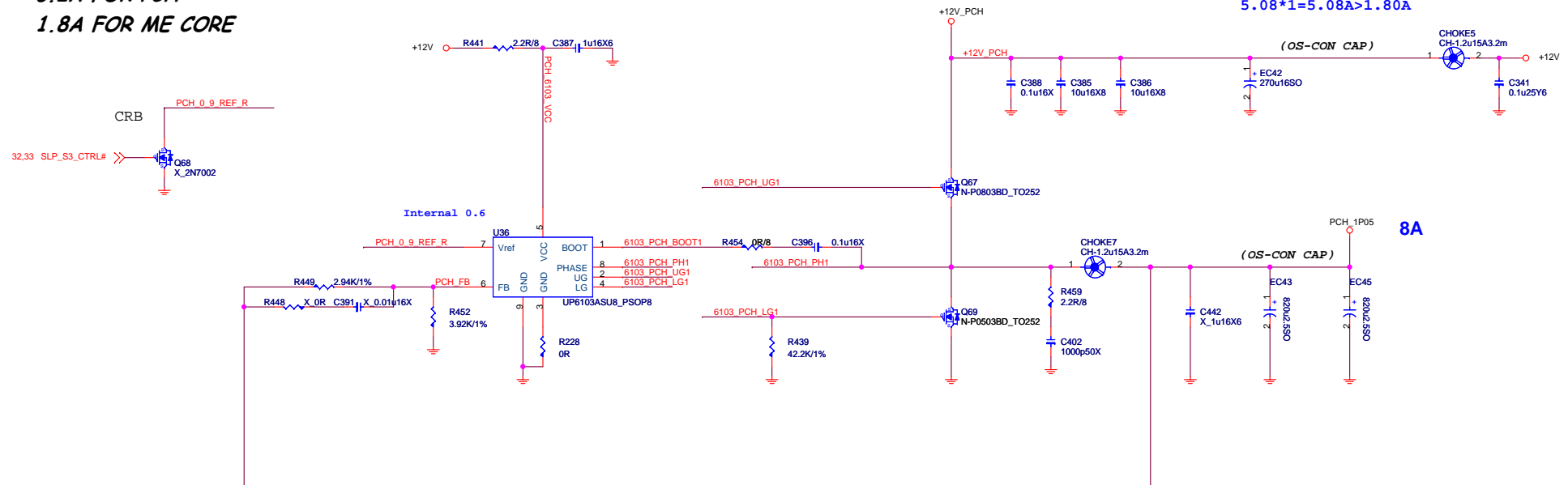
| | | |
|--------|----------------------------|----------------|
| Size | Document Description | Rev |
| Custom | DDR Power - uP6103 1-Phase | 2.0 |
| Date: | Sunday, January 23, 2011 | Sheet 29 of 39 |

PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE



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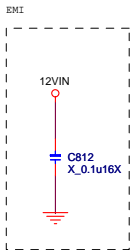
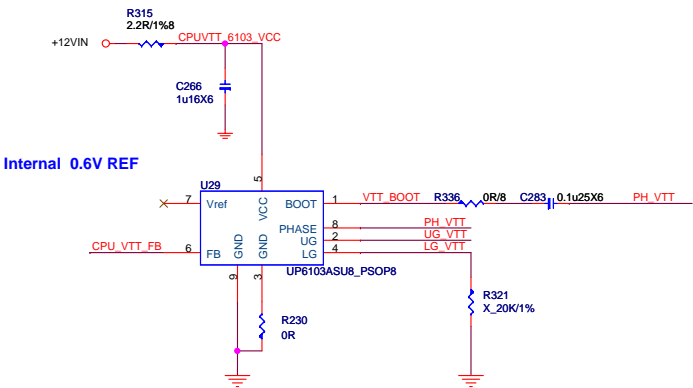
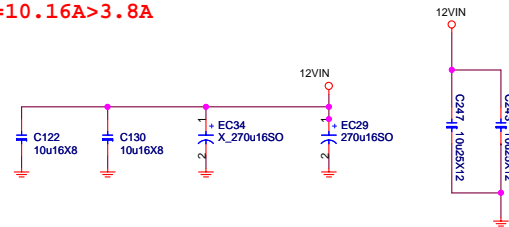
MS-7680

| Size | Document Description | Rev |
|--------|----------------------------|----------------|
| Custom | PCH Power - uP6103 1-Phase | 2.0 |
| Date: | Sunday, January 23, 2011 | Sheet 30 of 39 |

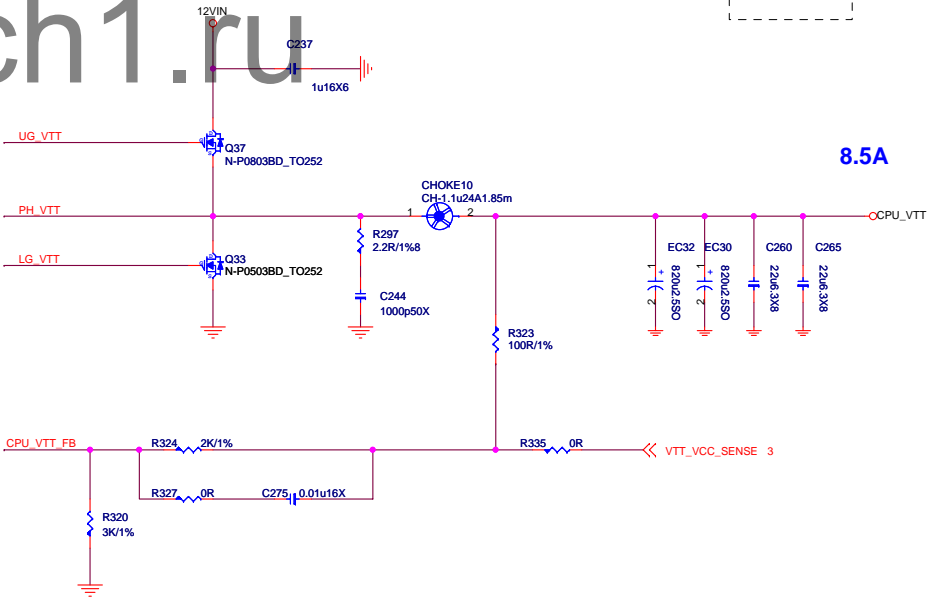
CPU_VTT:1.05/1.00

CPU VTT 8.5A + SA Core =8.8A =17.3A

$$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$$
$$5.08 * 2 = 10.16A > 3.8A$$

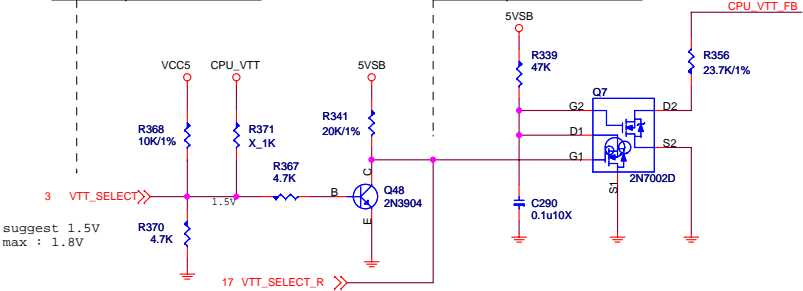


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| VTT_SELECT | |
|------------|-------|
| Low | 1.0V |
| High | 1.05V |

| VTT_SELECT Table | |
|------------------|-------|
| Low | 1.05V |
| High | 1.0V |



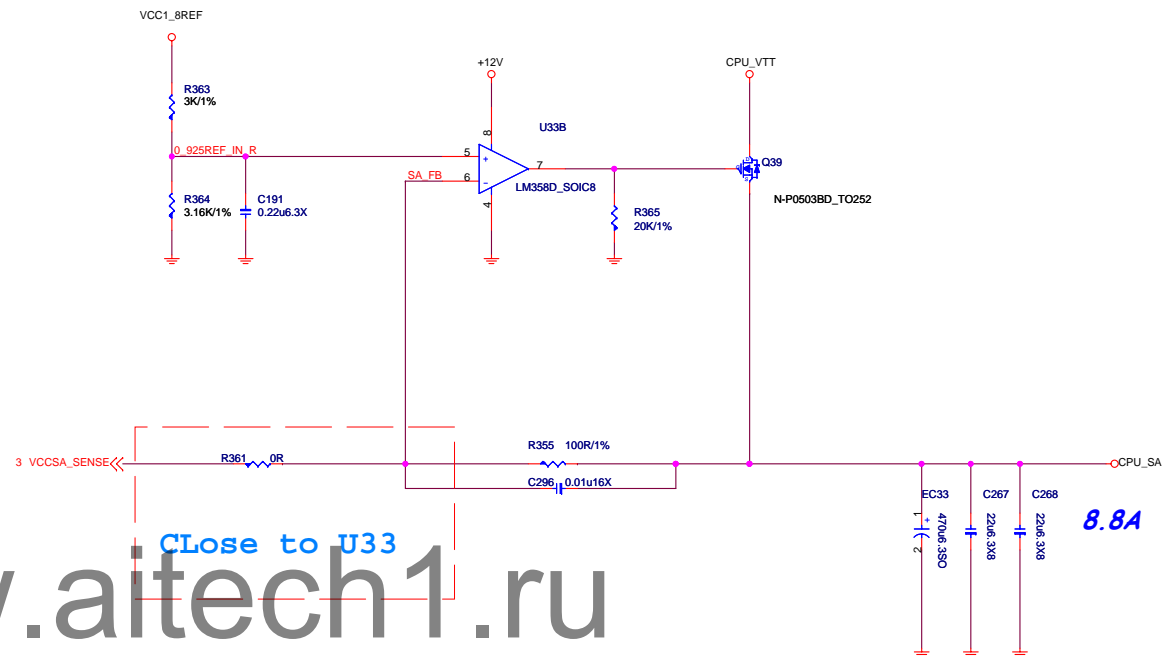
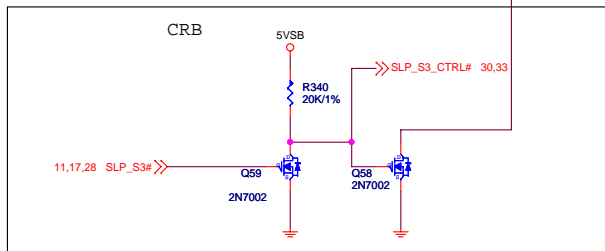
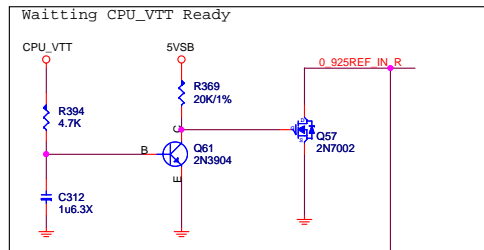
MICRO-STAR INT'L CO.,LTD

MS-7680

| Size | Document Description | Rev |
|--------|---------------------------|----------------|
| Custom | CPU_VTT - uP6103- 1-Phase | 2.0 |
| Date: | Sunday, January 23, 2011 | Sheet 31 of 39 |

CPU_SA:0.925/0.85

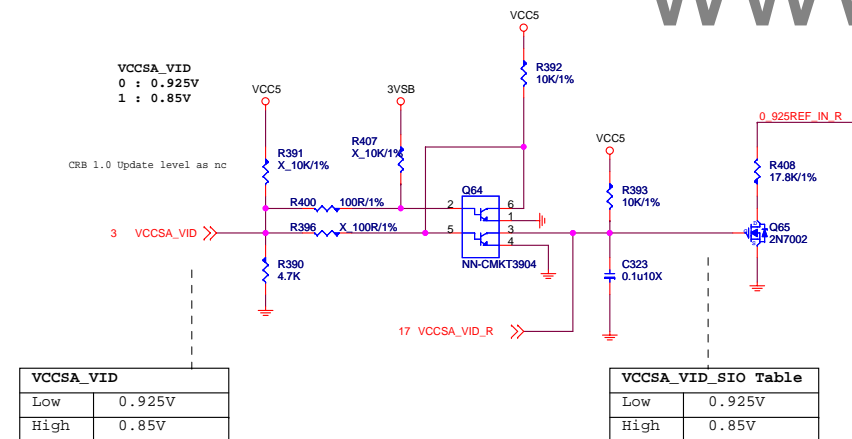
SA Core =8.8A



Close to U33

VCCSA_VID
0 : 0.925V
1 : 0.85V

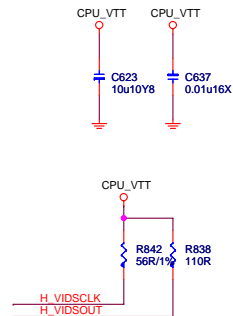
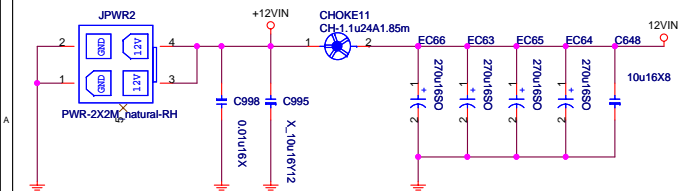
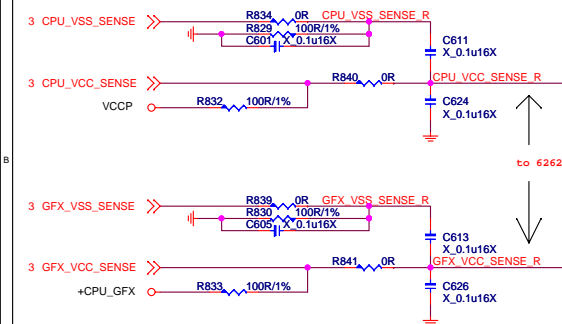
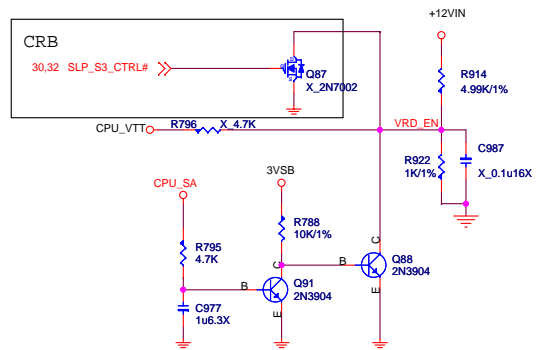
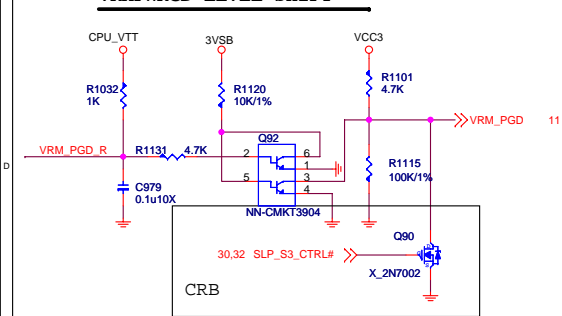
CRB 1.0 Update level as nc



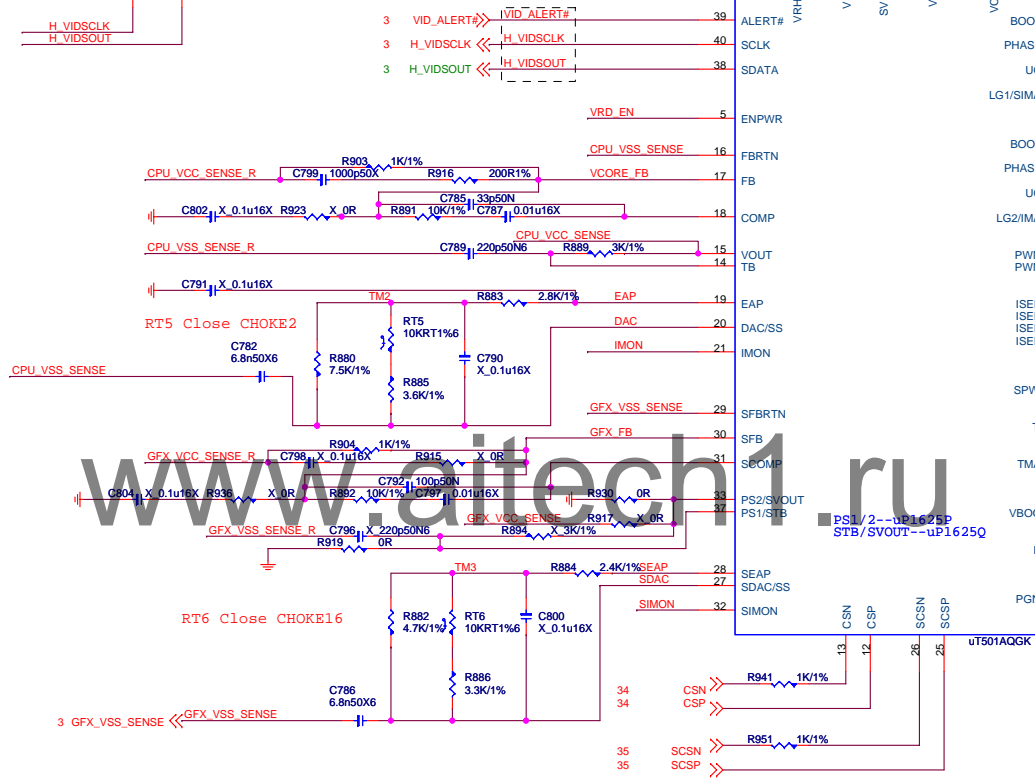
| VCCSA_VID | |
|-----------|--------|
| Low | 0.925V |
| High | 0.85V |

| VCCSA_VID_SIO Table | |
|---------------------|--------|
| Low | 0.925V |
| High | 0.85V |

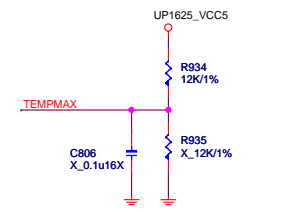
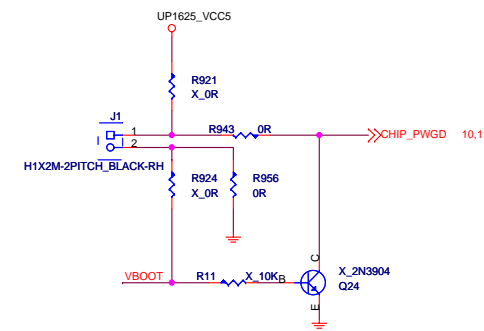
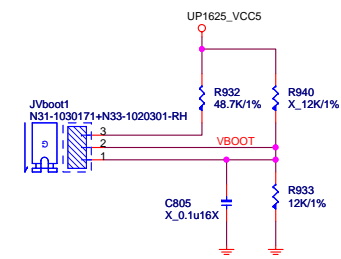
VRMPWRGD LEVEL SHIFT



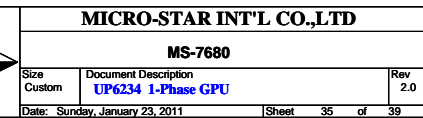
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



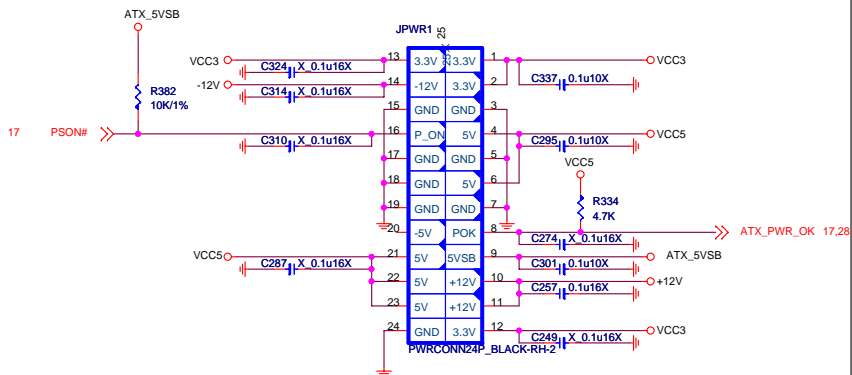
因為UP16250版本來不及趕上我們打板,所以先上P版本



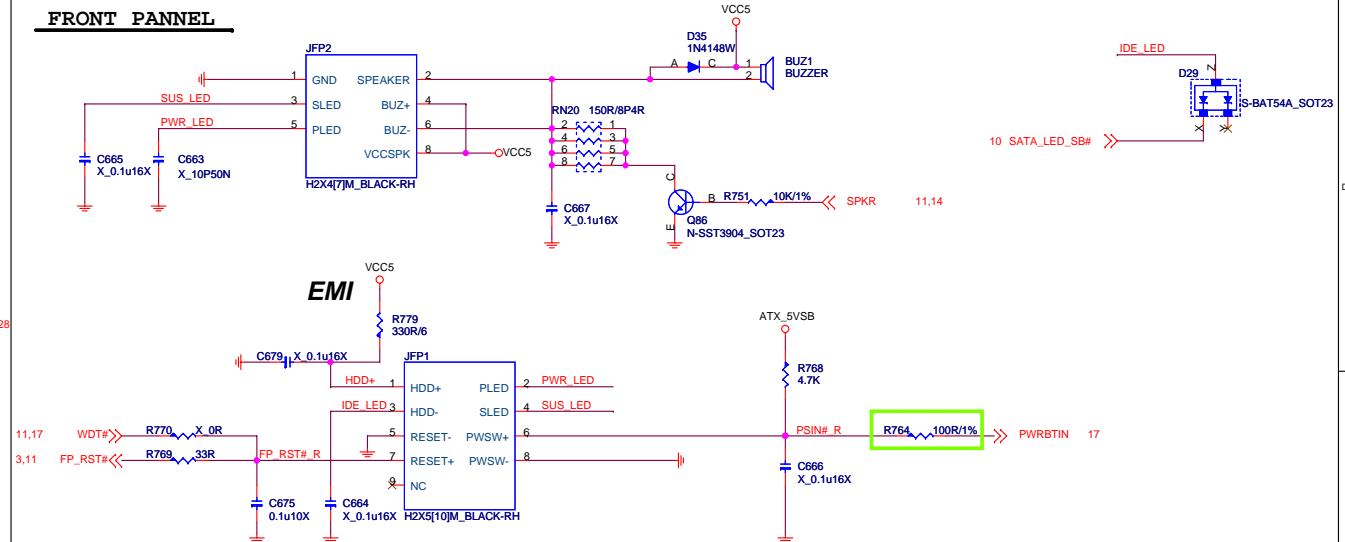
| MICRO-STAR INT'L CO.,LTD | | | |
|--------------------------|---------------------------|-------|----------|
| MS-7680 | | | |
| Size | Document Description | Rev | |
| Custom | VRD12 - UP16234 6+1-Phase | 2.0 | |
| Date: | Sunday, January 23, 2011 | Sheet | 33 of 39 |



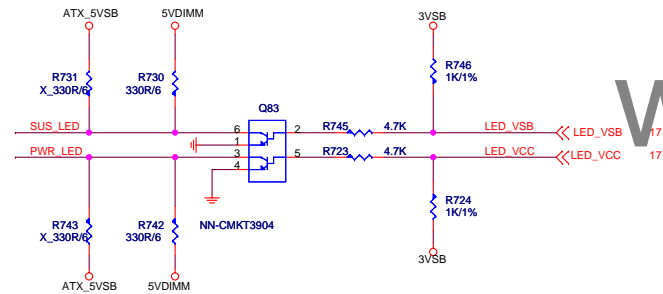
ATX POWER CONNECTOR



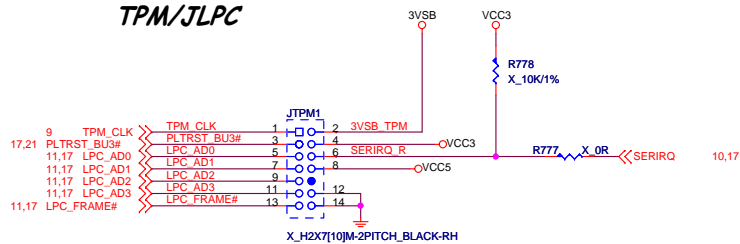
FRONT PANNEL



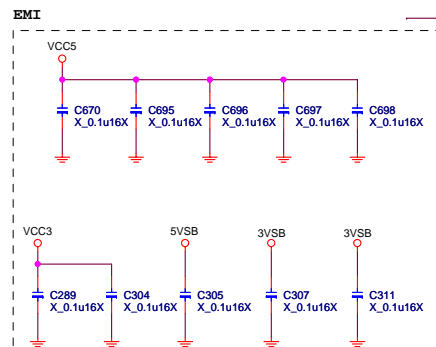
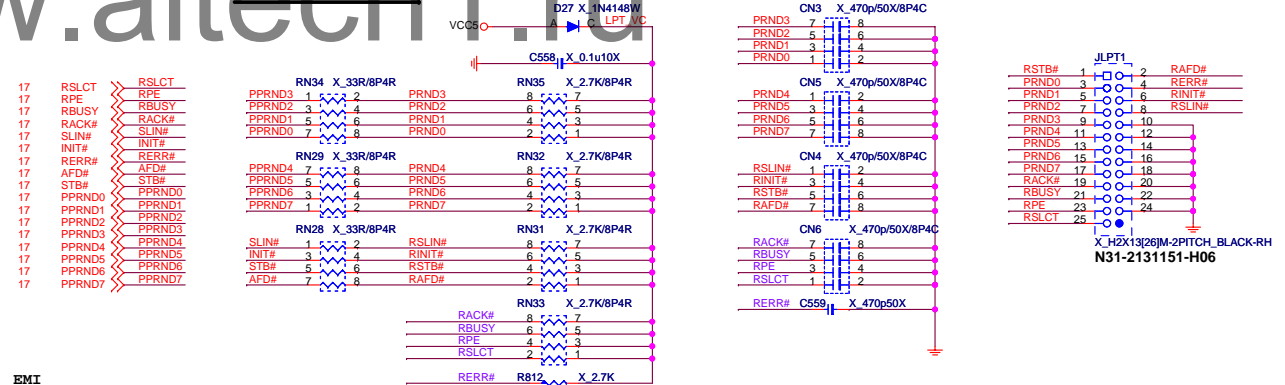
LED (for Fintek 71869)



TPM/JLPC



PARALLAL PORT



MICRO-STAR INT'L CO.,LTD

MS-7680

| | | |
|--------------------------------|--|----------------|
| Size Custom | Document Description ATX PWR-Connector & Front Panel & EMI | Rev 2.0 |
| Date: Sunday, January 23, 2011 | | Sheet 36 of 39 |

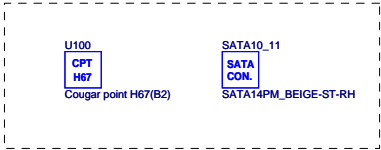
MS-7680-2.0

| OPT | Configure | BOM | Function |
|-----|------------------|--------------|--|
| A | CFG-7680-H61_E23 | 601-7680-02S | MS-7680 20 OPT:A H61M-E23 Intel H61+2*DDRIII+1*PCIE16,2*PCIE1,1*PCI+DVI/D-sub /HDMI+4*SATAII+10*USB2.0+HD8Ch Audio+Gb lan,EuP,(Half Solid Cap),RoHS |
| B | CFG-7680-H61_E35 | 601-7680-03S | MS-7680 20 OPT:B H61MU-E35 Intel H61+2*DDRIII+1*PCIE16,2*PCIE1,1*PCI+DVI/D-sub /HDMI+4*SATAII+2*USB3+10*USB2+HD8Ch Audio+Gb lan,EuP,(All Solid Cap),RoHS |
| C | CFG-7680-H67 | 601-7680-04S | MS-7680 20 OPT:B H67MU-E35 Intel H61+2*DDRIII+1*PCIE16,2*PCIE1,1*PCI+DVI/D-sub /HDMI+4*SATAII+2*USB3+10*USB2+HD8Ch Audio+Gb lan,EuP,(All Solid Cap),RoHS |

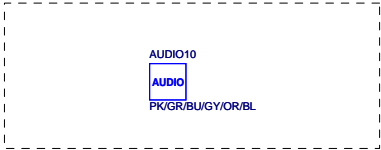
MS-7680-4.0

| OPT | Configure | BOM | Function |
|-----|----------------------|--------------|--|
| X | MS-7680-40 H61MU-S01 | 601-7680-XXX | MS-7680 40 H61MU-S01,H61+2DDR3+1*PCI_Ex16+3*PCI_Ex1+4*SATAII+HD 8CH Audio+10USB2.0+2USB3.0+Gb LAN, (EuP) ,RoHS |
| | | | |
| | | | |

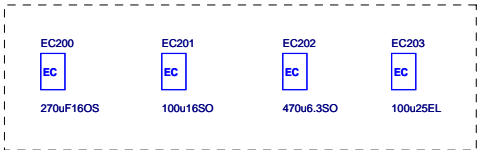
H67 OPT.



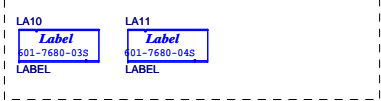
AUDIO CON OPT.



EL/OS OPT.



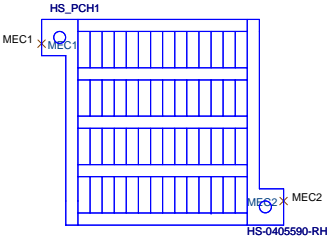
LABEL OPT.



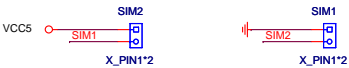
7680-20
PK0-0768020-G37, 精成, 23, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768020-G37, 精成, 32, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768020-E36, E&E, 23, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768020-E36, E&E, 22, 寶安恩斯通廠 (MSIS), 4, Coffee



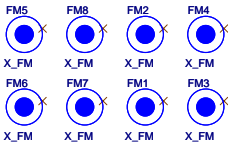
PCH XDP PWRGD/RESET



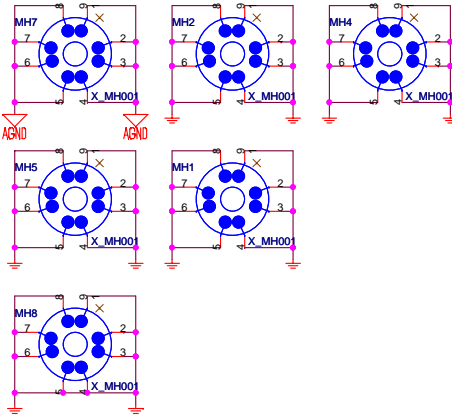
Simulation



Optical Fiducial Marks-120



Mounting Holes



| | | | |
|--------------------------------|----------------------|-------|----------|
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-7680 | | | |
| Size | Document Description | Rev | |
| Custom | XDP / Manual Parts | 2.0 | |
| Date: Sunday, January 23, 2011 | | Sheet | 37 of 39 |